ABSTRACT

In one embodiment, move buses utilized in presently known VLIW processors are eliminated and replaced with a busing scheme which results in transfer of operands from each register file bank to any data path block while also reducing the total bus width and total power consumption associated with transport of operands from register file banks to data path blocks. According to this busing scheme, the speed of VLIW processor is also improved since the need for one clock cycle to move operands from one register file bank to another is overcome. In another embodiment, a scheduling restriction is used to eliminate the need for the presently required write back buses used by various data path blocks. In yet another embodiment, a scheduling restriction is imposed which results in a reduction of the number of ports, a reduction in the width of buses, and a reduction of power consumption.